WEST

Help Logout Interrupt

Main Menu | Search Form | Posting Counts | Show S Numbers | Edit S Numbers | Preferences | Cases

Search Results -

Terms	Documents
L7 not l6	11

Database: US Patents Full-Text Database
US Pre-Grant Publication Full-Text Database
JPO Abstracts Database
EPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L8

Refine Search

Recall Text Clear

Search History

DATE: Tuesday, September 30, 2003 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
	DB=USPT,PGPB,JPAB,EPAB,DWPI,TDBD; PLUR=YES; OP=ADJ		
L8	L7 not l6	11	L8
L7	L4 and l5	19	L7
L6	L5 and l4 and l3	8	L6
L5	L2 same second order	20	L5
L4	L1 same first order	151	L4
L3	memory near3 (plurality or multiple or more than one) adj2 page	719	L3
L2	(data or image) adj3 destin$6	25967	L2
L1	(data or image) adj3 source	80413	L1

END OF SEARCH HISTORY

WEST

Generate Collection | Print

Search Results - Record(s) 1 through 11 of 11 returned.

☐ 1. Document ID: US 20030151609 A1

L8: Entry 1 of 11 File: PGPB Aug 14, 2003

DOCUMENT-IDENTIFIER: US 20030151609 A1
TITLE: Multi-sequence burst accessing for SDRAM

Detail Description Paragraph (21):
[0036] FIG. 5 is a block diagram of a data system 500. A data source 505 provides data to a scan converter system 510 in a first order. Scan converter system 510 includes a multi-sequence burst access SDRAM 512. SDRAM 512 has two sequences of burst accessing. Scan converter system 510 stores the data in SDRAM 512 according to the first order using a first sequence of burst accessing, as described above. Scan converter system 510 retrieves the data from SDRAM 512 in a second order using a second sequence of burst accessing and provides the retrieved data to a data destination 515.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw Desc | Image

☐ 2. Document ID: US 20020149596 A1

L8: Entry 2 of 11 File: PGPB Oct 17, 2002

DOCUMENT-IDENTIFIER: US 20020149596 A1
TITLE: Checkerboard buffer using more than two memory devices

Abstract Paragraph (1):
Methods and apparatus for storing and retrieving data in parallel but in different orders, using three or more memory devices. In one implementation, data for pixels is stored according to a checkered pattern, sequentially among memory devices, forming a checkerboard buffer. In one implementation, a checkerboard buffer includes: a data source, providing data in a first order; a data destination, receiving data in a second order; at least three memory devices each having memory locations, where data is stored in parallel to and retrieved in parallel from the memory devices; a first data switch connected to the data source and each of the memory devices, the first data switch controls which data is stored to which memory device; and a second data switch connected to the data destination and each of the memory devices, the second data switch controls providing data to the data destination according to the second order.

Summary of Invention Paragraph (22):
[0022] The present invention provides methods and apparatus for storing and retrieving data in parallel but in different orders, using three or more memory devices. In one implementation, data for pixels is stored according to a checkered pattern, sequentially among the memory devices, forming a checkerboard buffer. In one implementation, a checkerboard buffer includes: a data source, providing data in a first order; a data destination, receiving data in a second order; at least three memory devices, each memory device having a plurality of memory locations, where data is stored in parallel to the memory devices and retrieved in parallel from the memory devices; a first data switch connected to the data source and each of the memory devices, where the first data switch controls which data is stored to which memory device; and a second data switch connected to the data destination

and each of the memory devices, where the second data switch controls providing data to the data destination according to the second order.

Detail Description Paragraph (23):
[0073] FIG. 8 is a block diagram of a data system 800. A data source 805 provides data to a checkerboard buffer system 810 in a first order. Checkerboard buffer system 810 stores the data in a checkerboard pattern, as described above. Checkerboard buffer system 810 retrieves the data in a second order and provides the retrieved data to a data destination 815.

CLAIMS:

1. A checkerboard buffer, comprising: a data source, providing data in a first order; a data destination, receiving data in a second order; at least three memory devices, each memory device having a plurality of memory locations, where data is stored in parallel to the memory devices and retrieved in parallel from the memory devices; a first data switch connected to the data source and each of the memory devices, where the first data switch controls which data is stored to which memory device; and a second data switch connected to the data destination and each of the memory devices, where the second data switch controls providing data to the data destination according to the second order.

☐ 3. Document ID: US 20020113904 A1

L8: Entry 3 of 11 File: PGPB Aug 22, 2002

DOCUMENT-IDENTIFIER: US 20020113904 A1
TITLE: Two-dimensional buffer pages using bit-field addressing

Abstract Paragraph (1):
Methods and apparatus for storing data using two-dimensional arrays mapped to memory locations. In one implementation, a buffer page system includes: a data source, providing data elements in a first order; a data destination, receiving data elements in a second order; at least one memory device, each memory device having a plurality of memory pages including a plurality of memory locations, each memory location having an address; and where each data element corresponds to an entry in one of a plurality of buffer pages, where each buffer page has a plurality of entries along a first dimension corresponding to the first order and a plurality of entries along a second dimension corresponding to the second order, where data elements are stored according to the first order using blocks of buffer pages, each block having a number of buffer pages equal to a power of 2, where data elements are stored to the memory device in the first order and retrieved from the memory device in the second order, and where at least one memory page stores data elements in multiple locations according to the first order and stores data elements in multiple locations according to the second order.

Summary of Invention Paragraph (27):
[0027] The present disclosure provides methods and apparatus for storing data using two-dimensional arrays mapped to memory locations. In one implementation, a buffer page system includes: a data source, providing data elements in a first order; a data destination, receiving data elements in a second order; at least one memory device, each memory device having a plurality of memory pages including a plurality of memory locations, each memory location having an address; and where each data element corresponds to an entry in one of a plurality of buffer pages, where each buffer page has a plurality of entries along a first dimension corresponding to the first order and a plurality of entries along a second dimension corresponding to the second order, where data elements are stored according to the first order using blocks of buffer pages, each block having a number of buffer pages equal to a power of 2, where data elements are stored to the memory device in the first order and retrieved from the memory device in the second order, and where at least one memory page stores data elements in multiple locations according to the first order and stores data elements in multiple locations according to the second order.

Detail Description Paragraph (33):
[0098] FIG. 12 is a block diagram of a data system 1200. A data source 1205 provides data to a buffer page system 1210 in a first order. Buffer page system 1210 stores the data using buffer pages, as described above. Buffer page system 1210 retrieves the data in a second order and provides the retrieved data to a data destination 1215. For a video application, buffer page system 1210 can be used as a type of scan converter between data source 1205 and data destination 1215.

CLAIMS:

1. A buffer page system, comprising: a data source, providing data elements in a first order; a data destination, receiving data elements in a second order; at least one memory device, each memory device having a plurality of memory pages including a plurality of memory locations, each memory location having an address; and where each data element corresponds to an entry in one of a plurality of buffer pages, where each buffer page has a plurality of entries along a first dimension corresponding to the first order and a plurality of entries along a second dimension corresponding to the second order, where data elements are stored according to the first order using blocks of buffer pages, each block having a number of buffer pages equal to a power of 2, where data elements are stored to the memory device in the first order and retrieved from the memory device in the second order, and where at least one memory page stores data elements in multiple locations according to the first order and stores data elements in multiple locations according to the second order.

☐ 4. Document ID: US 20020110351 A1

DOCUMENT-IDENTIFIER: US 20020110351 A1
TITLE: Checkerboard buffer

Abstract Paragraph (1):
Methods and apparatus for storing and retrieving data in parallel but in different orders. In one implementation, data for pixels is stored according to a checkerboard pattern, alternately between two memory devices, forming a checkerboard buffer. In one implementation, a checkerboard buffer includes: a data source, providing data in a first order; a data destination, receiving data in a second order; at least two memory devices, each memory device having a plurality of memory locations, where data is stored in parallel to the memory devices and retrieved in parallel from the memory devices; a first data switch connected to the data source and each of the memory devices, where the first data switch controls which data is stored to which memory device; and a second data switch connected to the data destination and each of the memory devices, where the second data switch controls providing data to the data destination according to the second order.

Summary of Invention Paragraph (22):
[0022] The present invention provides methods and apparatus for storing and retrieving data in parallel but in different orders. In one implementation, data for pixels is stored according to a checkerboard pattern, alternately between two memory devices, forming a checkerboard buffer. In one implementation, a checkerboard buffer includes: a data source, providing data in a first order; a data destination, receiving data in a second order; at least two memory devices, each memory device having a plurality of memory locations, where data is stored in parallel to the memory devices and retrieved in parallel from the memory devices; a first data switch connected to the data source and each of the memory devices, where the first data switch controls which data is stored to which memory device; and a second data switch connected to the data destination and each of the memory devices, where the second data switch controls providing data to the data destination according to the second order.

Detail Description Paragraph (13):
[0066] FIG. 7 is a block diagram of a data system 700. A data source 705 provides data to a checkerboard buffer system 710 in a first order. Checkerboard buffer system 710 stores the data in a checkerboard pattern, as

described above. Checkerboard buffer system 710 retrieves the data in a second order and provides the retrieved data to a data destination 715.

CLAIMS:

1. A checkerboard buffer, comprising: a data source, providing data in a first order; a data destination, receiving data in a second order; at least two memory devices, each memory device having a plurality of memory locations, where data is stored in parallel to the memory devices and retrieved in parallel from the memory devices; a first data switch connected to the data source and each of the memory devices, where the first data switch controls which data is stored to which memory device; and a second data switch connected to the data destination and each of the memory devices, where the second data switch controls providing data to the data destination according to the second order.

55. A checkerboard buffer system, comprising: a data source, providing data in a first order; a data destination, receiving data in a second order; a checkerboard buffer, storing data from the data source in the first order and providing data to the data destination in the second order.

☐ 5. Document ID: US 20020109698 A1

L8: Entry 5 of 11 File: PGPB Aug 15, 2002

DOCUMENT-IDENTIFIER: US 20020109698 A1
TITLE: Checkerboard buffer using memory blocks

Abstract Paragraph (1):
Methods and apparatus for storing and retrieving data in parallel but in different orders. In one implementation, data for pixels is stored according to a checkerboard pattern, alternately between two memory devices, forming a checkerboard buffer. In one implementation, a checkerboard buffer includes: a data source, providing data in a first order; a data destination, receiving data in a second order; at least two memory devices, each memory device having a plurality of memory locations, where data is stored in parallel to the memory devices and retrieved in parallel from the memory devices, and where data is stored according to the first order using blocks of memory locations, each block having a number of memory locations equal to a power of 2; a first data switch connected to the data source and each of the memory devices, where the first data switch controls which data is stored to which memory device; and a second data switch connected to the data destination and each of the memory devices, where the second data switch controls providing data to the data destination according to the second order.

Summary of Invention Paragraph (23):
[0023] The present invention provides methods and apparatus for storing and retrieving data in parallel but in different orders. In one implementation, data for pixels is stored according to a checkerboard pattern, alternately between two memory devices, forming a checkerboard buffer. In one implementation, a checkerboard buffer includes: a data source, providing data in a first order; a data destination, receiving data in a second order; at least two memory devices, each memory device having a plurality of memory locations, where data is stored in parallel to the memory devices and retrieved in parallel from the memory devices, and where data is stored according to the first order using blocks of memory locations, each block having a number of memory locations equal to a power of 2; a first data switch connected to the data source and each of the memory devices, where the first data switch controls which data is stored to which memory device; and a second data switch connected to the data destination and each of the memory devices, where the second data switch controls providing data to the data destination according to the second order.

Detail Description Paragraph (13):
[0067] FIG. 7 is a block diagram of a data system 700. A data source 705 provides data to a checkerboard buffer system 710 in a first order. Checkerboard buffer system 710 stores the data in a checkerboard pattern, as

described above. Checkerboard buffer system 710 retrieves the data in a second order and provides the retrieved data to a data destination 715.

CLAIMS:

1. A checkerboard buffer, comprising: a data source, providing data in a first order; a data destination, receiving data in a second order; at least two memory devices, each memory device having a plurality of memory locations, where data is stored in parallel to the memory devices and retrieved in parallel from the memory devices, and where data is stored according to the first order using blocks of memory locations, each block having a number of memory locations equal to a power of 2; a first data switch connected to the data source and each of the memory devices, where the first data switch controls which data is stored to which memory device; and a second data switch connected to the data destination and each of the memory devices, where the second data switch controls providing data to the data destination according to the second order.

☐ 6. Document ID: US 20020109695 A1

L8: Entry 6 of 11 File: PGPB Aug 15, 2002

DOCUMENT-IDENTIFIER: US 20020109695 A1
TITLE: Checkerboard buffer using two-dimensional buffer pages and using state addressing

Abstract Paragraph (1):
Methods and apparatus for storing and retrieving data using two-dimensional arrays. In one implementation, a checkerboard buffer page system includes: a data source, providing data elements in a first order; a data destination, receiving data elements in a second order; memory devices each having memory pages, data elements stored in parallel to and retrieved in parallel from the memory devices; each buffer page having entries along a first dimension corresponding to the first order and entries along a second dimension corresponding to the second order, data elements stored in the first order and retrieved in the second order, at least one memory page stores data elements in multiple locations according to the first and second orders, at least two data elements consecutive in the first order stored in parallel, and where at least two data elements consecutive in the second order retrieved in parallel.

Summary of Invention Paragraph (27):
[0027] The present disclosure provides methods and apparatus for storing and retrieving data in parallel in two different orders using two-dimensional arrays mapped to memory locations. In one implementation, a checkerboard buffer page system includes: a data source, providing data elements in a first order; a data destination, receiving data elements in a second order; at least two memory devices, each memory device having a plurality of memory pages including a plurality of memory locations, each memory location having an address, where data elements are stored in parallel to the memory devices and retrieved in parallel from the memory devices; and where each data element corresponds to an entry in one of a plurality of buffer pages, each buffer page having a plurality of entries along a first dimension corresponding to the first order and a plurality of entries along a second dimension corresponding to the second order, and at least one entry in each buffer page corresponds to a data element, where data elements are stored to the memory devices in the first order and retrieved from the memory devices in the second order, and where at least one memory page stores data elements in multiple locations according to the first order and stores data elements in multiple locations according to the second order, where at least two data elements that are consecutive in the first order are stored in parallel to the memory devices, and where at least two data elements that are consecutive in the second order are retrieved in parallel from the memory devices.

Detail Description Paragraph (39):
[0100] FIG. 13 is a block diagram of a data system 1300. A data source 1305 provides data to a scan converter system 1310 in a first order. Scan converter system 1310 stores the data using a checkerboard buffer and buffer pages, as described above. Scan converter system 1310 retrieves the data in a second order and provides the

retrieved data to a data destination 1315. For a video application, scan converter system 1310 can be used as a type of scan converter between data source 1305 and data destination 1315.

CLAIMS:

1. A checkerboard buffer page system, comprising: a data source, providing data elements in a first order; a data destination, receiving data elements in a second order; at least two memory devices, each memory device having a plurality of memory pages including a plurality of memory locations, each memory location having an address, where data elements are stored in parallel to the memory devices and retrieved in parallel from the memory devices; and where each data element corresponds to an entry in one of a plurality of buffer pages, each buffer page having a plurality of entries along a first dimension corresponding to the first order and a plurality of entries along a second dimension corresponding to the second order, and at least one entry in each buffer page corresponds to a data element, where data elements are stored to the memory devices in the first order and retrieved from the memory devices in the second order, and where at least one memory page stores data elements in multiple locations according to the first order and stores data elements in multiple locations according to the second order, where at least two data elements that are consecutive in the first order are stored in parallel to the memory devices, and where at least two data elements that are consecutive in the second order are retrieved in parallel from the memory devices.

☐ 7. Document ID: US 20020109694 A1

L8: Entry 7 of 11 File: PGPB Aug 15, 2002

DOCUMENT-IDENTIFIER: US 20020109694 A1
TITLE: Checkerboard buffer using two-dimensional buffer pages and using bit-field addressing

Abstract Paragraph (1):
Methods and apparatus for storing and retrieving data. In one implementation, a system includes: a data source, providing data in a first order; a data destination, receiving data in a second order; memory devices having memory pages, data stored in parallel and retrieved in parallel; each buffer page having entries along a first dimension corresponding to the first order and entries along a second dimension corresponding to the second order, data stored according to the first order using blocks of buffer pages, each block having a number of pages equal to a power of 2, data stored in the first order and retrieved in the second order, at least one memory page stores data in multiple locations according to the first and second orders, data elements consecutive in the first order are stored in parallel, data elements consecutive in the second order are retrieved in parallel.

Summary of Invention Paragraph (28):
[0028] The present disclosure provides methods and apparatus for storing and retrieving data in parallel in two different orders using two-dimensional arrays mapped to memory locations. In one implementation, a checkerboard buffer page system includes: a data source, providing data elements in a first order; a data destination, receiving data elements in a second order; at least two memory devices, each memory device having a plurality of memory pages including a plurality of memory locations, each memory location having an address, where data elements are stored in parallel to the memory devices and retrieved in parallel from the memory devices; and where each data element corresponds to an entry in one of a plurality of buffer pages, each buffer page having a plurality of entries along a first dimension corresponding to the first order and a plurality of entries along a second dimension corresponding to the second order, where data elements are stored according to the first order using blocks of buffer pages, each block having a number of buffer pages equal to a power of 2, where data elements are stored to the memory devices in the first order and retrieved from the memory devices in the second order, and where at least one memory page stores data elements in multiple locations according to the first order and stores data elements in multiple locations according to the second order, where at least two data elements that are consecutive in the first order are stored in parallel to the memory devices, and where at least two data elements that are consecutive in the second order are retrieved in parallel from the memory devices.

Detail Description Paragraph (39):
[0103] FIG. 13 is a block diagram of a data system 1300. A data source 1305 provides data to a scan converter system 1310 in a first order. Scan converter system 1310 stores the data using a checkerboard buffer and buffer pages, as described above. Scan converter system 1310 retrieves the data in a second order and provides the retrieved data to a data destination 1315. For a video application, scan converter system 1310 can be used as a type of scan converter between data source 1305 and data destination 1315.

CLAIMS:

1. A checkerboard buffer page system, comprising: a data source, providing data elements in a first order; a data destination, receiving data elements in a second order; at least two memory devices, each memory device having a plurality of memory pages including a plurality of memory locations, each memory location having an address, where data elements are stored in parallel to the memory devices and retrieved in parallel from the memory devices; and where each data element corresponds to an entry in one of a plurality of buffer pages, each buffer page having a plurality of entries along a first dimension corresponding to the first order and a plurality of entries along a second dimension corresponding to the second order, where data elements are stored according to the first order using blocks of buffer pages, each block having a number of buffer pages equal to a power of 2, where data elements are stored to the memory devices in the first order and retrieved from the memory devices in the second order, and where at least one memory page stores data elements in multiple locations according to the first order and stores data elements in multiple locations according to the second order, where at least two data elements that are consecutive in the first order are stored in parallel to the memory devices, and where at least two data elements that are consecutive in the second order are retrieved in parallel from the memory devices.

☐ 8. Document ID: US 20020109691 A1

L8: Entry 8 of 11 File: PGPB Aug 15, 2002

DOCUMENT-IDENTIFIER: US 20020109691 A1
TITLE: Two-dimensional buffer pages using state addressing

Abstract Paragraph (1):
Methods and apparatus for storing data using two-dimensional arrays mapped to memory locations. In one implementation, a buffer page system includes: a data source, providing data elements in a first order; a data destination, receiving data elements in a second order; at least one memory device, each memory device having a plurality of memory pages including a plurality of memory locations, each memory location having an address; and where each data element corresponds to an entry in one of a plurality of buffer pages, where each buffer page has a plurality of entries along a first dimension corresponding to the first order and a plurality of entries along a second dimension corresponding to the second order, and at least one entry in each buffer page corresponds to a data element, where data elements are stored to the memory device in the first order and retrieved from the memory device in the second order, and where each memory page stores data elements in multiple locations according to the first order and stores data elements in multiple locations according to the second order.

Summary of Invention Paragraph (27):
[0027] The present disclosure provides methods and apparatus for storing data using two-dimensional arrays mapped to memory locations. In one implementation, a buffer page system includes: a data source, providing data elements in a first order; a data destination, receiving data elements in a second order; at least one memory device, each memory device having a plurality of memory pages including a plurality of memory locations, each memory location having an address; and where each data element corresponds to an entry in one of a plurality of buffer pages, where each buffer page has a plurality of entries along a first dimension corresponding to the first order and a plurality of entries along a second dimension corresponding to the second order, and at least one entry in each buffer page corresponds to a data element, where data elements are stored to the memory device in the first order

and retrieved from the memory device in the second order, and where each memory page stores data elements in multiple locations according to the first order and stores data elements in multiple locations according to the second order.

Detail Description Paragraph (33):
[0100] FIG. 12 is a block diagram of a data system 1200. A data source 1205 provides data to a buffer page system 1210 in a first order. Buffer page system 1210 stores the data using buffer pages, as described above. Buffer page system 1210 retrieves the data in a second order and provides the retrieved data to a data destination 1215. For a video application, buffer page system 1210 can be used as a type of scan converter between data source 1205 and data destination 1215.

CLAIMS:

1. A buffer page system, comprising: a data source, providing data elements in a first order; a data destination, receiving data elements in a second order; at least one memory device, each memory device having a plurality of memory pages including a plurality of memory locations, each memory location having an address; and where each data element corresponds to an entry in one of a plurality of buffer pages, where each buffer page has a plurality of entries along a first dimension corresponding to the first order and a plurality of entries along a second dimension corresponding to the second order, and at least one entry in each buffer page corresponds to a data element, where data elements are stored to the memory device in the first order and retrieved from the memory device in the second order, and where each memory page stores data elements in multiple locations according to the first order and stores data elements in multiple locations according to the second order.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC | Draw Desc | Image

9. Document ID: US 20020109690 A1

L8: Entry 9 of 11 File: PGPB Aug 15, 2002

DOCUMENT-IDENTIFIER: US 20020109690 A1
TITLE: Checkerboard buffer using memory bank alternation

Abstract Paragraph (1):
Methods and apparatus for storing and retrieving data in parallel but in different orders. In one implementation, data for pixels for one frame is stored according to a checkerboard pattern, alternately between two memory devices, forming a checkerboard buffer. While data is being stored, data for pixels from another frame is retrieved from another two memory devices. The banks of devices alternate between storing and retrieving with each frame. In one implementation, a checkerboard buffer includes: a data source, providing data in a first order; a data destination, receiving data in a second order; at least four memory devices, each memory device having a plurality of memory locations, where data is stored in parallel to at least two memory devices and retrieved in parallel from at least two memory devices; a first data switch connected to the data source and each of the memory devices, where the first data switch controls which data is stored to which memory device; and a second data switch connected to the data destination and each of the memory devices, where the second data switch controls providing data to the data destination according to the second order.

Summary of Invention Paragraph (23):
[0023] In one implementation, a checkerboard buffer includes: a data source, providing data in a first order; a data destination, receiving data in a second order; at least four memory devices, each memory device having a plurality of memory locations, where data is stored in parallel to at least two memory devices and retrieved in parallel from at least two memory devices; a first data switch connected to the data source and each of the memory devices, where the first data switch controls which data is stored to which memory device; and a second data switch connected to the data destination and each of the memory devices, where the second data switch controls providing data to the data destination according to the second order.

Detail Description Paragraph (13):
[0065] FIG. 7 is a block diagram of a data system 700. A data source 705 provides data to a checkerboard buffer system 710 in a first order. Checkerboard buffer system 710 stores the data in a checkerboard pattern, as described above. Checkerboard buffer system 710 retrieves the data in a second order and provides the retrieved data to a data destination 715.

CLAIMS:

1. A checkerboard buffer, comprising: a data source, providing data in a first order; a data destination, receiving data in a second order; at least four memory devices, each memory device having a plurality of memory locations, where data is stored in parallel to at least two memory devices and retrieved in parallel from at least two memory devices; a first data switch connected to the data source and each of the memory devices, where the first data switch controls which data is stored to which memory device; and a second data switch connected to the data destination and each of the memory devices, where the second data switch controls providing data to the data destination according to the second order.

☐ 10. Document ID: US 20020109689 A1

L8: Entry 10 of 11 File: PGPB Aug 15, 2002

DOCUMENT-IDENTIFIER: US 20020109689 A1
TITLE: Checkerboard buffer using sequential memory locations

Abstract Paragraph (1):
Methods and apparatus for storing and retrieving data in parallel but in different orders. In one implementation, data for pixels is stored according to a checkerboard pattern, alternately between two memory devices, forming a checkerboard buffer. In one implementation, a checkerboard buffer includes: a data source, providing data in a first order; a data destination, receiving data in a second order; at least two memory devices, each memory device having a plurality of memory locations, where data is stored in parallel to the memory devices and retrieved in parallel from the memory devices, and where data is stored according to the first order using sequential memory locations in the memory devices; a first data switch connected to the data source and each of the memory devices, where the first data switch controls which data is stored to which memory device; and a second data switch connected to the data destination and each of the memory devices, where the second data switch controls providing data to the data destination according to the second order.

Summary of Invention Paragraph (22):
[0022] The present invention provides methods and apparatus for storing and retrieving data in parallel but in different orders. In one implementation, data for pixels is stored according to a checkerboard pattern, alternately between two memory devices, forming a checkerboard buffer. In one implementation, a checkerboard buffer includes: a data source, providing data in a first order; a data destination, receiving data in a second order; at least two memory devices, each memory device having a plurality of memory locations, where data is stored in parallel to the memory devices and retrieved in parallel from the memory devices, and where data is stored according to the first order using sequential memory locations in the memory devices; a first data switch connected to the data source and each of the memory devices, where the first data switch controls which data is stored to which memory device; and a second data switch connected to the data destination and each of the memory devices, where the second data switch controls providing data to the data destination according to the second order.

Detail Description Paragraph (13):
[0066] FIG. 7 is a block diagram of a data system 700. A data source 705 provides data to a checkerboard buffer system 710 in a first order. Checkerboard buffer system 710 stores the data in a checkerboard pattern, as described above. Checkerboard buffer system 710 retrieves the data in a second order and provides the retrieved data to a data destination 715.

CLAIMS:

1. A checkerboard buffer, comprising: a data source, providing data in a first order; a data destination, receiving data in a second order; at least two memory devices, each memory device having a plurality of memory locations, where data is stored in parallel to the memory devices and retrieved in parallel from the memory devices, and where data is stored according to the first order using sequential memory locations in the memory devices; a first data switch connected to the data source and each of the memory devices, where the first data switch controls which data is stored to which memory device; and a second data switch connected to the data destination and each of the memory devices, where the second data switch controls providing data to the data destination according to the second order.

☐ 11. Document ID: EP 239269 A AU 8770520 A CA 1266534 A DE 3789912 G EP 239269 B1 US 4811411 A

L8: Entry 11 of 11 File: DWPI Sep 30, 1987

DERWENT-ACC-NO: 1987-272689
DERWENT-WEEK: 198739

TITLE: Virtual storage concept image processing system - stores data representing image on block basis where blocks represent image strips of virtual image

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments KWIC | Draw Desc | Image

Generate Collection Print

Terms	Documents
L7 not I6	11

Display Format: - Change Format

Set Name side by side	Query	Hit Count	Set Name result set
	DB=USPT,PGPB,JPAB,EPAB,DWPI,TDBD; PLUR=YES; OP=ADJ		
L11	L10 same buffer near2 page	0	L11
L10	frame near3 buffer same (parallel or concurren$4 or simultan$6) memory	26	L10
L9	frame near3 buffer same (parallel or concurren$4 or simultan$6) memory same stor$3 same (retriev$3 or recover$3 or fetch$3)	0	L9
L8	frame buffer same (parallel or concurren$4 or simultan$6) memory same stor$3 same (retriev$3 or recover$3 or fetch$3)	0	L8
L7	4647986[uref]	9	L7
L6	L5 not l4	1	L6
L5	L3 and l2	10	L5
L4	L3 same l2	9	L4
L3	memory adj6 (plurality or multiple or more than one or various or numerous) adj3 location	3493	L3
L2	(plurality or multiple or more than one or various or numerous) adj3 buffer near2 page	155	L2
L1	(plurality or multiple or more than one or various or numerous) adj3 buffer page	19	L1

END OF SEARCH HISTORY

WEST

Help Logout Interrupt

Main Menu | Search Form | Posting Counts | Show S Numbers | Edit S Numbers | Preferences | Cases

Search Results -

Terms	Documents
L10 same buffer near2 page	0

Database: US Patents Full-Text Database
US Pre-Grant Publication Full-Text Database
JPO Abstracts Database
EPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L11

Refine Search

Recall Text Clear

Search History

DATE: Tuesday, September 30, 2003 Printable Copy Create Case

Search Results - Record(s) 1 through 26 of 26 returned.

1. Document ID: US 20030126351 A1

L10: Entry 1 of 26 File: PGPB Jul 3, 2003

DOCUMENT-IDENTIFIER: US 20030126351 A1
TITLE: Conflict-free memory system and method of address calculation and data routing by using the same

Summary of Invention Paragraph (20):
[0018] Tables 1(a) and 1(b) show the class of storage schemes, linearity, routing method, subarray types, constant intervals, the hardware implementation, simultaneity, location of access, the burden to the PE's, and the number of memory modules of the previous memory systems and the memory system proposed in the present invention for the SIMD processor to fulfill the goals (1).about.(6) by using a linear skewing scheme, (1) D. T. Harper III, "Block, Multistride Vector, and FFT Accesses in Parallel Memory Systems," IEEE Trans. Parallel Distrib. Sys., vol. 2, pp. 43-51, January 1991; (2) D. T. Harper III, "Increased Memory Performance during Vector Accesses through the Use of Linear Address Transformations," IEEE Trans. Comput., vol. C-41, pp. 227-230, February 1992; (3) W. Oed and O. Lange, "On the Effective Bandwidth of Interleaved Memories in Vector Processing Systems," IEEE Trans. Comput., vol. C-34, pp. 949-957, October 1985; (4) D. T. Harper III and J. R. Jump, "Vector Access Performance in Parallel Memories Using a Skewed Storage Scheme," IEEE Trans. Comput., vol. C-36, pp. 1440-1449, December 1987; (5) R. Raghavan and J. P. Hayes, "On Randomly Interleaved Memories," Supercomputing '90, pp. 49-58, 1990; (6) K. Batcher, "The Multidimensional Access Memory in STARAN," IEEE Trans. Comput., I vol 26, no. 1, pp. 174-177, 1977; (7) J. Frailong, W. Jalby, and J. Lenfant, "XOR-schemes: A Flexible Data Organization in Parallel Memories," in Proc. Int. Conf. Parallel Processing, pp. 276-283, 1985; (8) A. Norton and E. Melton, "A Class of Boolean Linear Transformations for Conflict-free Power-of-two Stride Access," in Proc. Int. Conf. Parallel Processing, pp. 247-254, 1987; (9) D. Lee, "Scrambled Storage for Parallel Memory Systems," in Proc. Int. Symp. on Comp. Architecture, pp. 232-239, 1988; (10) K. Kim and V. K. P. Kumar, "Perfect Latin Squares and Parallel Array Access," in Proc. Int. Symp. on Comp. Architecture, pp. 372-379, 1989; (11) C. S. Raghavendra and R. Boppana, "On Methods for Fast and Efficient Parallel Memory Access," in Proc. Int. Conf. Parallel Processing, pp. 76-83, 1990; (12) 32. D. T. Harper III, "A Multiaccess Frame Buffer Architecture," IEEE Trans. Comput., Vol. C-43, pp. 618-622, May 1994; (13) P. Budnik and D. J. Kuck, "The Organization and Use of Parallel Memories," IEEE Trans. Comput., vol. C-20, pp. 1566-1569, December 1971; (14) H. Wijshoff and J. Van Leeuwen, "On Linear Skewing Schemes and d-ordered Vectors," IEEE Trans. Comput., vol. C-36, no. 2, pp. 233-239, February 1987 (15) D. H. Lawrie, "Access and Alignment of Data in an Array Processor." IEEE Trans. Comput., vol. C-24, no. 12, pp. 1145-1155, December 1975; (16) D. C. Van Voorhis and T. H. Morrin, "Memory Systems for Image Processing," IEEE Trans. Comput., vol. C-27, pp. 113-125, February 1978; (17) J. W. Park, "An Efficient Memory System for Image Processing," IEEE Trans. Comput., vol. C-35, pp. 669-674, July 1986; "An Efficient Memory System for Image Processing," Korean Patent No. 32719 (1990); "Memory System for Image Processing Having Address Calculating Circuitry Permitting Simultaneous Access to Block, Horizontal Sequence and Vertical Sequence Subarrays of an Array Data," U.S. Pat. No. 4,926,386 (1990); (18) D. H. Lawrie and C. R. Vora, "The Prime Memory System for Array Access," IEEE Trans. Comput., vol. C-31, pp. 435-442, May 1982; (19) D. T. Harper III and D. A. Linebarger, "Conflict-free Vector Access Using a Dynamic Storage Scheme," IEEE Trans. Comput., vol. C-40, no. 3, pp. 276-283, March 1991; (20) A Deb, "Multiskewing--A Novel Technique for Optimal Parallel Memory Access," IEEE Trans. Parallel Distrib. Syst., Vol. 7, No. 6, pp. 595-604, June 1996; (21) J. W. Park and D. T. Harper III, "Memory Architecture Support for the SIMD Construction of a Gaussian Pyramid," IEEE Symp. Parallel and Distributed Processing, pp. 444-451, December 1992; (22) J. W. Park and D. T. Harper III, "An Efficient Memory System for the Construction of a Gaussian pyramid," IEEE Trans. Parallel Distrib. Syst., vol. 7, No. 8, pp. 855-860, August 1996; (23) J. W. Park, "Efficient Image Analysis and Processing Memory System," Korean Patent No. 58542 (1993); "Efficient Image Analysis and Processing Memory System," Japanese Patent No. 2884815 (2000); (24) J. W. Park, "Multi-access Memory System with the Constant Interval for Image Processing," Korean Patent No. 121295 (1997).

☐ 2. Document ID: US 20030095124 A1

L10: Entry 2 of 26 File: PGPB May 22, 2003

DOCUMENT-IDENTIFIER: US 20030095124 A1
TITLE: Back-end image transformation

Detail Description Paragraph (46):
[0066] In addition to memory access requests generated by pixel processing logic 501, frame buffer 402 also gets memory access requests from external sources. For this reason, memory arbiter & timing control logic 920 is used to determine the priority of concurrent memory access requests that may occur and generate the required memory control signals. Memory arbiter & timing control logic 920 receives as inputs MemoryClock signal for clocking, OtherMemoryRequest signal, and ScreenRequest signal. ScreenRequest signal is the output of AND-gate 919 which receives as inputs ScreenRequestStop signal and FifoNotFull signal from Screen FIFO 918. Screen FIFO 918 provides a buffer for a plurality of data words received from frame buffer 402 before outputting it on ScreenFifoData[63:0] signal to pixel processing logic 408. Hence, Screen FIFO 918 asserts a FifoNotFull signal when it has one or more empty locations to ask memory arbiter & timing control for the next 64-bits data word in the line. FifoNotFull signal and ScreenRequestStop signal are both provided as inputs to AND-gate 919 which asserts ScreenRequest signal only if Screen FIFO 918 is empty and there is more data in the line to access. Otherwise, AND-gate 919 deasserts ScreenRequest signal. Memory arbiter & timing control 920 generates a ScreenRequestAck signal which is provided to Screen FIFO 918 in response to a ScreenRequest signal and an OtherMemoryAck signal in response to an OtherMemoryRequest signal. Memory arbiter & timing control circuit 920 then generates MemoryAddressSelect signal to select the proper memory address to access frame buffer 402. If memory arbiter & timing control 920 decides that the memory access is on behalf of Screen FIFO 918 (ScreenRequest) then the MemoryAddressSelect signal will indicate to MemoryAddressTranslation 910 to select ScreenAddress[17:0] and output of adders 907-909 as addresses for memory modules M0-M3 of frame buffer 402. If memory arbiter & timing control 920 decides that the memory access is on behalf of OtherMemoryRequest then the MemoryAddressSelect signal will indicate to MemoryAddressTranslation 910 to select OtherMemoryAddress as addresses for frame buffer 402. Memory arbiter & timing control 920 also generates memory read/write controls and clock signals to perform the actual read or write access to the frame buffer memory 402. In response to frame buffer 402 read access due to ScreenRequest, frame buffer 402 provides 64-bits of image data related to each accessed memory read on memory read data bus MRD[63:0] to Screen FIFO 918. Concurrently, memory arbiter & timing control 920 asserts ScreenRead signal to latch the 64-bits data provided by MRD[63:0] into Screen FIFO 918. When Screen FIFO 918 receives an asserted ScreenFifoRead signal from pixel serialization logic 501, screen FIFO 918 reads from the next FIFO location and outputs the content on ScreenFifoData[63:0] signal. Screen FIFO 918 also synchronizes the reception of both ScreenRead signal and ScreenFifoRead signal with MemoryClock signal to update FifoNotFull signal.

☐ 3. Document ID: US 20020009293 A1

L10: Entry 3 of 26 File: PGPB Jan 24, 2002

DOCUMENT-IDENTIFIER: US 20020009293 A1
TITLE: HDTV video server

Detail Description Paragraph (17):

[0039] In a currently preferred embodiment of the present invention, processor system 50 may be an SGI 4-node Origin 2000 platform, chosen for it's high-speed XIO bus 34. Frame buffer 28 may be an SGI XT-HD frame buffer suitable for its outstanding RGB conversion ability, especially in light of its capability to deliver the desired RGB12 packing mode. Multiple processor cards 51 provide more memory nodes 54 that enable parallel memory access. Fiber Channel interface boards 52 were chosen for their ease of use and high throughput. Other suitable components may be used.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC | Draw Desc | Image

---

☐ 4. Document ID: US 6233361 B1

L10: Entry 4 of 26 File: USPT May 15, 2001

DOCUMENT-IDENTIFIER: US 6233361 B1
TITLE: Topography processor system

Detailed Description Text (16):
The dedicated output buffers are cleared in the frame period following their particular output cycle which necessitates triple buffering of these physically and logically partitioned parallel memories.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC | Draw Desc | Image

---

☐ 5. Document ID: US 6184907 B1

L10: Entry 5 of 26 File: USPT Feb 6, 2001

DOCUMENT-IDENTIFIER: US 6184907 B1
TITLE: Graphics subsystem for a digital computer system

Detailed Description Text (18):
Memory controller 150 controls the frame buffer 220 (see FIG. 1) in response to the memory read request signal M_RQ such that data of 3.times.4 (=q).times.64(=r) bits, which corresponds to first scan blocks SB(i-1,1), SB(i,1) and SB(i+1,1) of three adjacent scan lines SL.sub.i-1, SL.sub.i and SL.sub.i+1, is sequentially and successively read from the frame buffer 220 while the display enable signal D_EN remains inactivated. Simultaneously, the memory controller 150 generates the write enable signal W_EN to instruct the FIFO buffer 140 to store the data output from the frame buffer 220. Subsequently, data corresponding to second scan blocks SB(i-1,2), SB(i,2) and SB(i+1,2) of the three adjacent scan lines SL.sub.i-1, SL.sub.i and SL.sub.i+1, (where, i=1, 2, . . . , or n) are also sequentially and successively read from the frame buffer 220 and written into the FIFO buffer 140. The remaining scan blocks SB(1,3), SB(1,4), . . . , SB(n,p) (see FIG. 3B) in the frame buffer 220 are also fed to the FIFO buffer 140 in the same manner.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC | Draw Desc | Image

---

☐ 6. Document ID: US 5867180 A

L10: Entry 6 of 26 File: USPT Feb 2, 1999

DOCUMENT-IDENTIFIER: US 5867180 A
TITLE: Intelligent media memory statically mapped in unified memory architecture

Detailed Description Text (8):
On the other hand, the UMA has been known to have a performance problem when the computer system start to require more graphic performance and higher resolution displays. This is because the access to the memory containing a frame-buffer is much more frequent compared to others even though all of the memory access go through the same single memory port. Historically, this bandwidth requirement has been driving to separate the frame-buffer from the main memory. This severe bandwidth requirement in the UMA system is expected to be even worse in the near future. For example, a Super extended Graphics Array (SXGA)display, having a resolution of 1200.times.1024 pixels and 24 bits per pixel, will require more than 300 MB only for a screen refresh and more than one gigabyte (1 GB) for simultaneous memory accesses including operations of three dimensional (3D) graphics and motion pictures. It is important to note that this memory bandwidth requirement is asymmetrically distributed along the memory space. In other words, the memory bandwidth requirement is only for the specific memory address space related to the screen operations while for other memory address spaces where ordinary programs and data are stored, the bandwidth requirement is not as severe. In addition, the memory bandwidth problem in the UMA is further exasperated by the overhead resulting from the bus arbitration due to simultaneous memory accesses from multiple resources such as CPU, graphic accelerator, and so on.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments

KWIC | Draw Desc | Image

☐ 7. Document ID: US 5822768 A

L10: Entry 7 of 26

File: USPT

Oct 13, 1998

DOCUMENT-IDENTIFIER: US 5822768 A
TITLE: Dual ported memory for a unified memory architecture

Brief Summary Text (14):
In one embodiment, the serial controller is a graphics controller that utilizes part of the dual ported memory as a frame buffer. The remaining portion of the dual ported memory is used as system memory. To execute a screen refresh operation, the graphics controller generates the serial port load command to receive serial data via the serial port. The dual ported memory transmits data from the serial port, and it permits concurrent memory access via the random access port. Thus, screen refresh operations may be executed concurrent to memory access requests by a memory master device, such as a central processing unit, a peripheral device or a serial controller.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments

KWIC | Draw Desc | Image

☐ 8. Document ID: US 5805133 A

L10: Entry 8 of 26

File: USPT

Sep 8, 1998

DOCUMENT-IDENTIFIER: US 5805133 A
**** See image for Certificate of Correction ****
TITLE: Method and apparatus for increasing the rate of scrolling in a frame buffer system designed for windowing operations

Abstract Text (1):

A frame buffer including a memory array, circuitry for accessing the array, a plurality of latches each capable of storing a plurality of pixel values equivalent to a large portion of a row of pixels in the array which may be read simultaneously from the array, and circuitry for writing simultaneously to the memory cells of a row of the array the data stored in the latches whereby a row of pixels may be read and written back to the array bus in a minimum time period.

Brief Summary Text (12):
These and other objects of the present invention are realized in a frame buffer including a memory array, circuitry for accessing the array, a plurality of latches each capable of storing a plurality of pixel values equivalent to a large portion of a row of pixels in the array which may be read simultaneously from the array, and circuitry for writing simultaneously to the memory cells of a row of the array the data stored in the latches whereby a row of pixels may be read and written back to the array bus in a minimum time period.

9. Document ID: US 5646693 A

L10: Entry 9 of 26 File: USPT Jul 8, 1997

DOCUMENT-IDENTIFIER: US 5646693 A
TITLE: Memory utilization for video decoding and display with 3:2 pull-down

Detailed Description Text (81):
During the decoding of the last row of macroblocks for which image information for both fields is written to frame buffer 38 concurrently, memory controller 22 notifies parser 14 that, beginning with the next row of macroblocks, the frame will be decoded twice by asserting store bitstream location signal 56. This signal is sampled by parser 14 between rows of macroblocks. When signal 56 is asserted, parser 14 stores the location of the beginning of the slice at the beginning of the next row of macroblocks in register 28.

10. Document ID: US 5602780 A

L10: Entry 10 of 26 File: USPT Feb 11, 1997

DOCUMENT-IDENTIFIER: US 5602780 A
TITLE: Serial to parallel and parallel to serial architecture for a RAM based FIFO memory

Detailed Description Text (2):
Before discussing with particular detail a preferred embodiment of the invention as illustrated in FIG. 2, FIG. 1 first illustrates an example of a data transmission system wherein the invention may be advantageously employed. Data transmission system 2 includes a unique memory buffer 4 coupling a first transmission device 6 to a second transmission device 8. As will be explained in further detail below, memory buffer 4 includes a novel random access memory (RAM) based first-in, first out (FIFO) memory architecture that advantageously implements serial to parallel and parallel to serial conversions. When writing to the memory buffer, data bits are input serially into a write frame buffer where they are temporarily stored in data latches until the buffer fills whereupon the bits are written in parallel to the memory array, thus providing a serial to parallel conversion. When reading from memory buffer 4, a number of bits are accessed from the memory array in parallel and are input into a read frame buffer where they are stored temporarily in data latches until they are thereafter clocked out serially, thus providing a parallel to serial conversion. Such architecture advantageously provides a one bit wide FIFO where a data word is only one bit wide.

☐ 11. Document ID: US 5596540 A

L10: Entry 11 of 26

File: USPT

Jan 21, 1997

DOCUMENT-IDENTIFIER: US 5596540 A
TITLE: Serial to parallel and parallel to serial architecture for a RAM based FIFO memory

Detailed Description Text (2):
Before discussing with particular detail a preferred embodiment of the invention as illustrated in FIG. 2, FIG. 1 first illustrates an example of a data transmission system wherein the invention may be advantageously employed. Data transmission system 2 includes a unique memory buffer 4 coupling a first transmission device 6 to a second transmission device 8. As will be explained in further detail below, memory buffer 4 includes a novel random access memory (RAM) based first-in, first out (FIFO) memory architecture that advantageously implements serial to parallel and parallel to serial conversions. When writing to the memory buffer, data bits are input serially into a write frame buffer where they are temporarily stored in data latches until the buffer fills whereupon the bits are written in parallel to the memory array, thus providing a serial to parallel conversion. When reading from memory buffer 4, a number of bits are accessed from the memory array in parallel and are input into a read frame buffer where they are stored temporarily in data latches until they are thereafter clocked out serially, thus providing a parallel to serial conversion. Such architecture advantageously provides a one bit wide FIFO where a data word is only one bit wide.

☐ 12. Document ID: US 5533187 A

L10: Entry 12 of 26

File: USPT

Jul 2, 1996

DOCUMENT-IDENTIFIER: US 5533187 A
TITLE: Multiple block mode operations in a frame buffer system designed for windowing operations

Abstract Text (1):
A frame buffer having a memory array, circuitry for accessing the array, a plurality of color value registers for storing a plurality of color values which may be written to the array, and circuitry for writing to the memory cells a data representing a single pixel, for writing simultaneously to the memory cells data representing a number of pixels equal to the number of conductors on the data bus, or for writing simultaneously to the memory cells data representing an entire row of pixels of the array.

Brief Summary Text (17):
These and other objects of the present invention are realized in a frame buffer having a memory array, circuitry for accessing the array, a plurality of color value registers for storing a plurality of color values which may be written to the array, and circuitry for writing simultaneously to the memory cells representing an entire row of pixels of the array in selected color modes and to selected adjacent groups of pixels whereby an entire row of a window may be written in a minimum number of accesses.

☐ 13. Document ID: US 5170468 A

L10: Entry 13 of 26

File: USPT

Dec 8, 1992

DOCUMENT-IDENTIFIER: US 5170468 A
TITLE: Graphics system with shadow ram update to the color map

Detailed Description Text (52):
The first function of the address refinement mechanism is bank selection. Recall that in the actual preferred embodiment the frame buffer 25 is organized into banks zero (groups A-D) and one (groups E-H). In this organization the pairs of groups A/E, B/F, C/G and D/H each receive their own address and bank select lines. The pairs rely upon the bank select lines to distinguish between otherwise identical addresses that might be sent to a pair. For example, to access the 16.times.1 tile 33 of FIGS. 5A and 7, simultaneous memory cycles to groups C and D of bank 0 and to E and F of bank 1 are required. This situation will produce at the output of latch 51 zeros for the signals CG.sub.-- SEL and DH.sub.-- SEL, and ones for the signals AE.sub.-- SEL and BF.sub.-- SEL. Those signals are the bank select lines actually used by the frame buffer memory 25.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments

KWIC | Draw Desc | Image

☐ 14. Document ID: US 5131080 A

L10: Entry 14 of 26

File: USPT

Jul 14, 1992

DOCUMENT-IDENTIFIER: US 5131080 A
TITLE: Graphics frame buffer with RGB pixel cache

Detailed Description Text (52):
The first function of the address refinement mechanism is bank selection. Recall that in the actual preferred embodiment the frame buffer 25 is organized into banks zero (groups A-D) and one (groups E-H). In this organization the pairs of groups A/E, B/F, C/G and D/H each receive their own address and bank select lines. The pairs rely upon the bank select lines to distinguish between otherwise identical addresses that might be sent to a pair. For example, to access the 16.times.1 tile 33 of FIGS. 5A and 7, simultaneous memory cycles to groups C and D of bank 0 and to E and F of bank 1 are required. This situation will produce at the output of latch 51 zeros for the signals CG.sub.-- SEL and DH.sub.-- SEL, and ones for the signals AE.sub.-- SEL and BF.sub.-- SEL. Those signals are the bank select lines actually used by the frame buffer memory 25.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments

KWIC | Draw Desc | Image

☐ 15. Document ID: US 5056044 A

L10: Entry 15 of 26

File: USPT

Oct 8, 1991

DOCUMENT-IDENTIFIER: US 5056044 A
TITLE: Graphics frame buffer with programmable tile size

Detailed Description Text (52):
The first function of the address refinement mechanism is bank selection. Recall that in the actual preferred

embodiment the frame buffer 25 is organized into banks zero (groups A-D) and one (groups E-H). In this organization the pairs of groups A/E, B/F, C/G and D/H each receive their own address and bank select lines. The pairs rely upon the bank select lines to distinguish between otherwise identical addresses that might be sent to a pair. For example, to access the 16.times.1 tile 33 of FIGS. 5A and 7, simultaneous memory cycles to groups C and D of bank 0 and to E and F of bank 1 are required. This situation will produce at the output of latch 51 zeros for the signals CG.sub.-- SEL and DH.sub.-- SEL, and ones for the signals AE.sub.-- SEL and BF.sub.-- SEL. Those signals are the bank select lines actually used by the frame buffer memory 25.

CLAIMS:

7. A method of addressing a frame buffer having a plurality of planes, representing a pixel address space and containing multi-bit pixel values, to access in unison a tile of contiguous pluralities of pixels, the method comprising the steps of:

a. addressing K-many separately addressable N-bit groups of RAM, each N-bit group for reading and writing N-bit words during K-many simultaneous memory cycles with separate addresses for each N-bit group, K being an integer greater than or equal to two and N being an integer greater than or equal to one, the K-many N-bit groups forming a plane of the multi-plane frame buffer, each such plane having a data path of (KN)-many bits arranged as an ordering by group of the K-many N-bit groups;

b. repeating step (a) once for each plane in the frame buffer, there being one such plane for each bit of a multi-bit pixel value;

c. forming a tile address including a separate address for each N-bit group, each separate address being a function of at least the pixel address and the N-bit group with which that separate address is associated; and

d. for each plane in the frame buffer, performing simultaneous memory cycles upon each N-bit group with the separate addresses of the tile address, whereby a tile of (KN)-many multi-bit pixel values is accessed in the space of a single memory cycle.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments

KWIC | Draw Desc | Image

☐ 16. Document ID: US 5029105 A

L10: Entry 16 of 26

File: USPT

Jul 2, 1991

DOCUMENT-IDENTIFIER: US 5029105 A
TITLE: Programmable pipeline for formatting RGB pixel data into fields of selected size

Detailed Description Text (52):
The first function of the address refinement mechanism is bank selection. Recall that in the actual preferred embodiment the frame buffer 25 is organized into banks zero (groups A-D) and one (groups E-H). In this organization the pairs of groups A/E, B/F, C/G and D/H each receive their own address and bank select lines. The pairs rely upon the bank select lines to distinguish between otherwise identical addresses that might be sent to a pair. For example, to access the 16.times.1 tile 33 of FIGS. 5A and 7, simultaneous memory cycles to groups C and D of bank 0 and to E and F of bank 1 are required. This situation will produce at the output of latch 51 zeros for the signals CG.sub.-- SEL and DH.sub.-- SEL, and ones for the signals AE.sub.-- SEL and BF.sub.-- SEL. Those signals are the bank select lines actually used by the frame buffer memory 25.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments

KWIC | Draw Desc | Image

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments KWIC | Draw Desc | Image

☐ 22. Document ID: US 4517597 A

L10: Entry 22 of 26 File: USPT May 14, 1985

DOCUMENT-IDENTIFIER: US 4517597 A
TITLE: Method and apparatus for encoding and decoding video

Detailed Description Text (24):
A modulo 24 counter 1231 counts decoder memory output clock pulses, which are at a higher rate (for example, twice the rate in this embodiment) than the decoder memory input clocks. The output of the modulo 24 counter 1231 is used as a strobe signal to strobe the 24 pixels in parallel from the memories 1121, 1122, 1123, and 1124 into their respective output buffer registers 1221, 1222, 1223, and 1224. The output of the modulo 24 counter 1231 is also coupled to the input of the modulo 24 counter 1232 whose count is utilized as the sequence address to the four memories 1121, 1122, 1123 and 1124. The output of modulo 24 counter 1232 is coupled to a modulo 482 counter 1233 whose count is utilized as a line address to the memories 1121, 1122, 1123 and 1124. Accordingly, during each frame period, the memories 1121, 1122, 1123 and 1124 output, from their respective buffers, the latest stored frames of I, X, Y and Z information. As described, the I information is "updated" every frame, and the X, Y and Z difference signal information is "updated" every three frames, so the outputs X, Y and Z are each read out three times redundantly before "new" information is read out.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments KWIC | Draw Desc | Image

☐ 23. Document ID: JP 01267600 A

L10: Entry 23 of 26 File: JPAB Oct 25, 1989

DOCUMENT-IDENTIFIER: JP 01267600 A
TITLE: BUFFER MEMORY

Abstract Text (1):
PURPOSE: To enable conversion in mutually different data array formats in a bit map type frame buffer space by providing a 1st serial port for inputting data from X-directionally parallel memory cells in parallel and a 2nd serial port for inputting Y-directional data in parallel.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments KWIC | Draw Desc | Image

☐ 24. Document ID: WO 9512191 A1

L10: Entry 24 of 26 File: EPAB May 4, 1995

PUB-NO: WO009512191A1
DOCUMENT-IDENTIFIER: WO 9512191 A1
TITLE: METHOD FOR INCREASING THE RATE OF SCROLLING IN A FRAME BUFFER

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments KWIC | Draw Desc | Clip Img | Image

☐ 25. Document ID: KR 340621 B WO 9512166 A1 EP 677192 A1 US 5533187 A EP 677192 A4 JP 09506440 W EP 677192 B1 DE 69425426 E

L10: Entry 25 of 26 File: DWPI Oct 11, 2002

DERWENT-ACC-NO: 1995-215031
DERWENT-WEEK: 200325

TITLE: Frame buffer for windowing operations - writes simultaneously to memory cells representing entire row of pixels of array in selected colour modes and selected adjacent groups of pixels

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC | Draw Desc | Clip Img | Image

☐ 26. Document ID: WO 8906033 A CA 1312393 C DE 3850389 G EP 348479 A EP 348479 B1 JP 04501777 W US 4935880 A

L10: Entry 26 of 26 File: DWPI Jun 29, 1989

DERWENT-ACC-NO: 1989-206746
DERWENT-WEEK: 198928

TITLE: SIMD graphics system with figure tilting facility - accesses frame buffer arrays and determines if figure extends to arrays above or below accessed array, and tests position of each sample

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC | Draw Desc | Image

Generate Collection | Print

Terms	Documents
frame near3 buffer same (parallel or concurren$4 or simultan$6) memory	26

Display Format: - Change Format

Previous Page Next Page